# Whole Chip ESD Protection

This Application is a DIV of 10/205529 7/25/2002 US Patent 6,730,968

## Background of the Invention

### Field of the Invention

This invention relates to a whole chip electrostatic discharge, ECD, circuit and method.

In particular, this invention relates to distributing the circuit of this invention next to each input / output pad in order to provide parallel ESD current discharge paths.

### Description of Related Art

Figure 1 shows a prior art input/output protection circuit. This protection circuit is placed next to each input/output (I/O) pad. Each protection circuit, like the one shown in figure 1, is used to protect only one I/O pad. If one of the I/o pads is zapped with high voltage or high current, the electrostatic discharge, ESD, current 170 only flows through the protection circuit adjacent to the zapped I/o pad. The circuit in figure 1 is connected to the supply voltage Vcc 190 and to Vss 150 or ground. The circuit includes a p-channel metal oxide semiconductor field effect transistor PMOS FET device 110 and an n-channel metal oxide